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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,020	06/29/2006	Masahiro Kubota	283380US2PCT	3989

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
04/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/563,020	KUBOTA ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7 and 8* is/are rejected.

7)☒ Claim(s) *2,3 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/28/2006 was considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4-5, 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda (U.S. Patent No. 6,734,863).

As per claim 1, as shown in Fig. 1, Ikeda teaches a video signal processing circuit, comprising:

a GRAM (VRAM 4) *which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal* (col. 9, lines 7-19);

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM (col. 9, lines 20-24); and

a control unit (VRAM arbitration circuit 8),

wherein said pixel data corresponding to said pixels representing said scanning line stored in said latch circuit is displayed on said display screen (col. 9, lines 20-34), *and*

in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control unit delays for a predetermined delay time reading of said pixel data corresponding to said pixels representing said scanning line and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again (col. 5, lines 41-54, i.e. arbitrating access to VRAM (8) between rewriting detection circuit 7 (writing to pixel data to VRAM) and refresh control circuit (reading to scan line from VRAM), i.e. a delay time when the rewriting detection circuit 7 has access right to VRAM 4, and when the refresh control unit 10 get the access right to the VRAM, it can perform the reading from GRAM to the latch circuit again, see also disclosure of Figs. 3 and 4).

As per claim 4, Ikeda inherently teaches *said control means unit comprises a monitoring means unit which monitors whether writing of said pixel data in said GRAM contends against reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM* (i.e. monitoring the access right between the rewriting detection circuit 7 and the refresh control circuit 10, see col. 5, lines 41-54).

As per claim 5, as cited above in claims 1 and 4, Ikeda also teaches *said control means unit comprises a delay means unit which delays reading of said pixel data corresponding to said pixels representing said scanning line based on a monitoring result obtained by said monitoring*

means unit and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

Claims 7 and 8, which are similar in scope to claim 1, are thus rejected under the same rationale.

Allowable Subject Matter

4. Claims 2, 3 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art taken singly or in combination does not teach or suggest, a video signal processing circuit, among other things, comprising

*said control means unit comprises a delay unit which delays and inputs a display read control signal and a data latch signal for said predetermined delay time during a period which is after a point at which said memory clock signal corresponding to writing of said pixel data in said GRAM is supplied, said writing accompanying said contention, but which is before supplying of the next memory clock signal following said memory clock signal so that said latch circuit reads pixel data corresponding to pixels representing said scanning lin*e (claim 2);

when writing of said pixel data in said GRAM is executed plural times during a contention-free memory update period in which said pixel data corresponding to said pixels representing said scanning line are read to said latch circuit from said GRAM said control means unit upon occurrence of said contention delays reading of said pixel data corresponding to said pixels representing said scanning line between a period of writing said pixel data and a

period of writing next pixel data, and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM again plural times during said contention-free memory update period (claim 6).

The closest prior art, Ikeda (U.S. Patent No. 6,734,863) fails to teach the above features.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

/Hau H Nguyen/

Examiner, Art Unit 2628